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Tracce per domande orali

1. Quali sono le principali topologie circuitali per i circuiti di front-end a basso rumore per la lettura di segnali provenienti da rivelatori di radiazione? Descriverne brevemente i principi di funzionamento, le caratteristiche principali ed i vantaggi e svantaggi di ciascuno.

2. Definire la Carica Equivalente di Rumore (ENC, Equivalent Noise Charge) in un sistema di rivelazione costituito da un sensore di radiazione e dalla relativa elettronica di front-end e si discutano i contributi principali al rumore elettronico nel sistema.

3. Descrivere l'impatto dello scaling sul design di circuiti integrati analogici, digitali e mxed-signal per rivelatori di radiazione, descrivendo per i vari tipi di circuiti vantaggi e svantaggi dell'uso di tecnologie fortemente scalate.

4. Discutere come alcune caratteristiche e performance richieste nell'ambito di un particolare esperimento impiegante rivelatori e relativa elettronica di front-end orientino la scelta verso un determinato tipo di ADC.

5. Descrivere il flusso di progetto per un sistema di acquisizione dati basato su FPGA in esperimenti di fisica che necessitino di alta velocità di lettura dei dati di un sistema di rivelazione multicanale.

All.3

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TIGER: A front-end ASIC for timing and energy measurements with radiation detectors

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ABSTRACT

A mixed-signal ASIC for timing and energy measurements with radiation detectors is described. The chip embeds 64 channels, each of which features a charge-sensitive amplifier followed by a dual-shaper coupled to low-offset discriminators. A versatile back-end, incorporating low-power Time to Digital Converters and Wilkinson Analog to Digital Converters with derandomizing buffers allows to encode both the time of arrival and the charge of the input signal. The ASIC is designed for a maximum detector capacitance of 100 pF and an event rate in excess of 60 kHz per channel. A peak detector samples the input signal with an excellent linearity in the range 5 ÷ 55 fC. Charge digitization with Time-over-Threshold is also supported to extend the dynamic range. Fabricated in a 110 nm CMOS process, the chip dissipates 10 mW/channel. The ASIC was primarily developed to readout the cylindrical GEM detector of the BESIII experiment. For its characteristics it can serve however a broad class of radiation sensors, including silicon microstrip detectors.

Contents

1. Introduction

TIGER (Turin Integrated Gem Electronics Readout) is a 64-channel mixed-signal ASIC that allows simultaneous time and energy measurements with radiation detectors. The chip has been primarily developed to readout the Cylindrical Gas Electron Multiplier detector (CGEM), a novel ultra-light weight tracker to be installed in the inner part of the BESIII experiment, a tau-charm factory exploiting the Beijing e^+e^- collider BEPCII [1].

Fig. 1 shows a conceptual design of the CGEM detector, which is formed by three independent concentric layers, covering 93% of the solid angle. Each layer is in turn composed by five cylindrical structures: one cathode, three GEM foils and the readout anode. One GEM foil is made of a layer of 50 μm Kapton, copper clad on each side and with a high density of bi-conical holes. The holes have an inner diameter of 50 μm and an outer diameter of 70 μm. Inside each hole, an electric field of 100 kV/cm multiplies the number of primary electrons to achieve a detectable signal. The triple GEM structure is chosen because it allows to reach high gain with a minimum discharge probability.

Embedded in a 1 T magnetic field, the new tracker must provide a momentum resolution of 0.5% at 1 GeV and a rate capability of 10 kHz/cm^2 . A spatial resolution of 120 μm in the direction transverse to the beam and of 1 mm in the longitudinal one is targeted. The total

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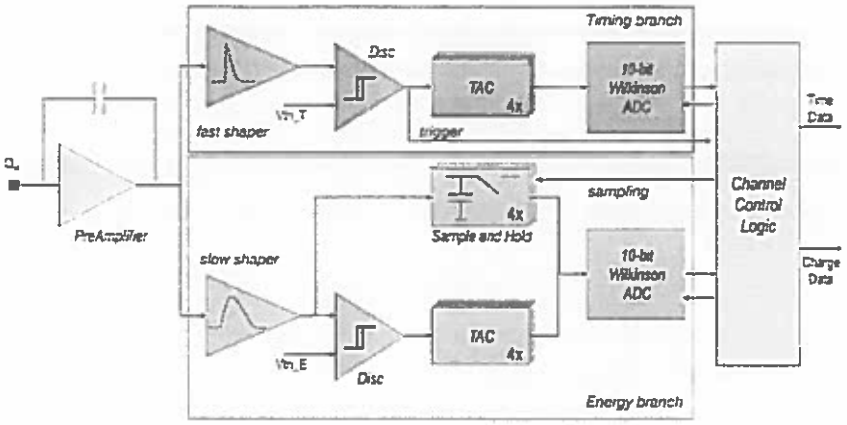

Fig. 2. Block diagram of one ASIC channel.

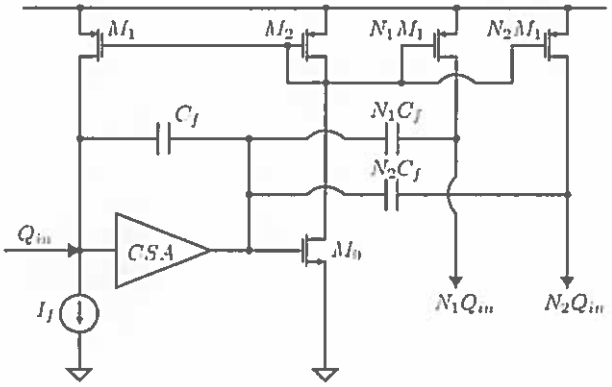

Fig. 3. Channel input stage.

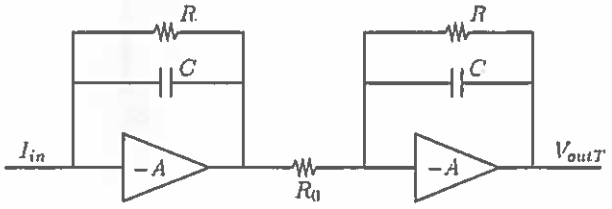

Fig. 4. Shaper used in the timing branch.

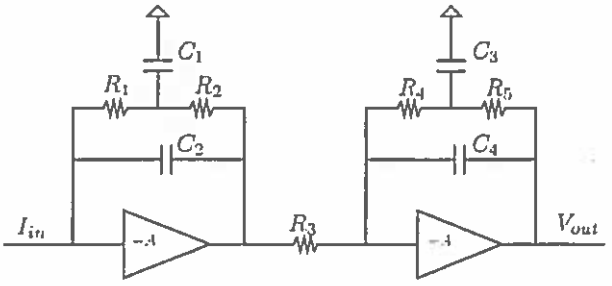

Fig. 5. Shaper used in the energy branch.

The coarse time information is obtained by counting the transitions of the chip master clock, that can be up to 200 MHz. The TAC is employed to interpolate the time elapsing between the hit detection flagged by the discriminator and a suitable clock edge. The analogue voltage of each TAC is then digitized by the Wilkinson ADC with a maximum resolution of 10 bits. To make the interpolation robust against metastability in the digital logic, a time corresponding to 1.5 times the master clock period is measured, therefore a minimum binning of 7.3 ps is possible, resulting in a maximum conversion time of 5.12 μs . Increasing the time bin reduces the conversion time accordingly. For instance, measuring the interpolation time with a 7 bit resolution results in a binning of 60 ps and a maximum conversion time of 640 ns. The slope of the TDC is controlled with a 6 bit DAC implemented on board of the ASIC and can thus be adjusted according to the operation needs. Four TACs are available for derandomization purposes [8,9], therefore the TDC can accommodate an event rate in excess of 1 MHz with an efficiency better than 99%. The rate capability is thus mainly limited by pulse pile-up in the front-end amplifier. An array of four capacitors allows to sample and hold the peak voltage at the output of the slow shaper. The stored voltage is digitized by a second Wilkinson ADC, which is shared with the TDC serving the energy branch.

The chip operation is supervised by a digital controller [10,11]. This unit generates all the digital signals necessary to drive the sample and hold (S&H), the TDC and the Wilkinson ADC and manages the chip configuration and the data transmission to the outside world. Each hit generates a 64 bit word, which can be transmitted over one of the four serial LVDS links in 32 clock cycles thanks to the Double Data Rate (DDR) operation. With a clock frequency of 200 MHz, the total output bandwidth is 1.6 Gbit/s. This allows to transmit $2.5 \cdot 10^7$ events/s, which is equivalent to a frequency of 391 kHz/channel. Triple Modular Redundancy (TMR) is employed to protect critical registers against Single Event Upsets (SEU). The technology was tested by another research group up to Total Ionizing Dose (TID) of 5 Mrad, which is much above the maximum dose expected in BESIII. Minimal degradation were observed [12], so a standard layout approach has been adopted.

Thanks to the hardware resources deployed in each channel, the chip offers different operating modes, briefly described hereafter.

Time-over-threshold (tot). In this mode, the leading and trailing edge of the discriminator are captured by the TDCs. The charge is thus inferred from the measured pulse duration. The ToT readout allows to extend the charge sensitivity beyond the saturation point of the front-end amplifier (50 fC nominal). In principle, either discriminator can be chosen, even though the one following the fast shaper provides more accurate timing information and it is thus the default choice in this mode.

Peak sampling. the output of the discriminator connected to the fast shaper provides a trigger to the control logic, which generates a sampling pulse with a delay suitable to capture the slow shaper output around its maximum. The delay between the trigger and the sampling pulse can be fine-tuned in steps equal to four clock cycles. For a 10 bit

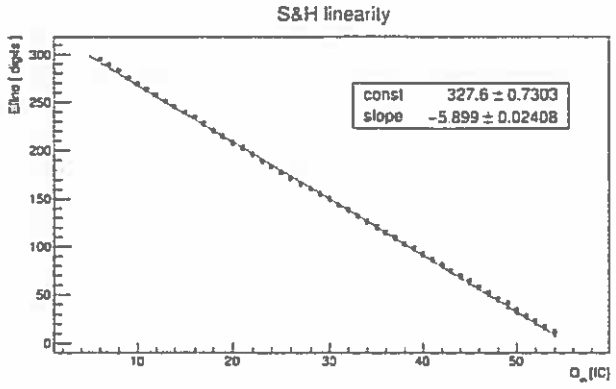

Fig. 10. S&H ADC output as a function of the input charge.

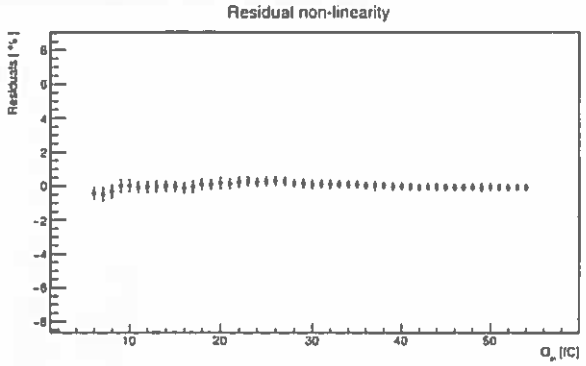

Fig. 11. Front-end nonlinearity.

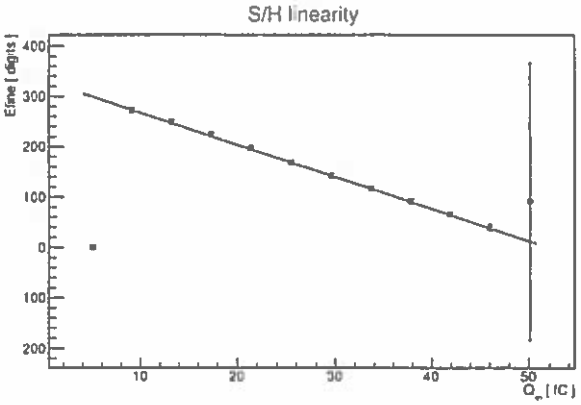

Fig. 12. Linearity plot obtained with the test pulse generator integrated on chip.

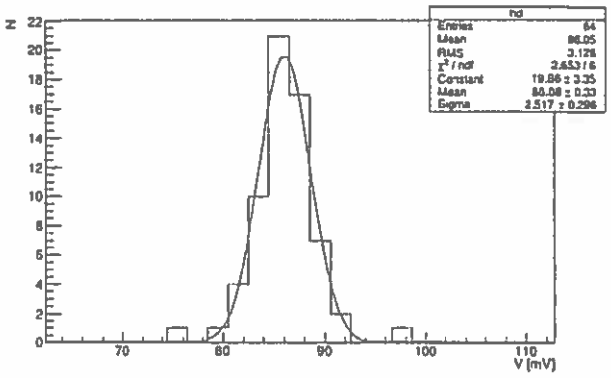

Fig. 13. Gain distribution of all channels on one ASIC, obtained for an input charge of 8 fC.

detail the observed non-linearity profile was not pursued. Test signals can be fed to the amplifier input by the test pulse generator integrated on chip, which allows to selectively address all the channels in the ASIC. The resulting linearity plot is shown in Fig. 12. It can be seen from the figure that significant deviations from linearity are observed at the edges of the dynamic range. This is attributed to the fact that signal amplitude is defined by regulating a current and for very small or very high values of this current some of the transistors in the pulse generator work outside the saturation region. While this point can be easily fixed in a next release of the ASIC by properly re-sizing the critical devices, the circuit is suitable to assess the basic functionality of the individual channels, whereas a linearity test to explore the full dynamic range with sufficient granularity must be performed with an external signal source.

The performance of the very front-end can also be assessed with S-curve measurements. Fig. 13 displays the gain of all 64 channels on one ASIC, measured through this method. In the test, an input signal of 8 fC is injected. The threshold is scanned, till the signal peak is found by detecting the 50% triggering point. The baseline in then subtracted to obtain the net peak amplitude. An average peak amplitude of 86 mV is measured, which corresponds to a gain of 10.76 mV/fC, which is very close to the 11 mV/fC expected from post-layout simulations.The RMS variation is 3.1 mV which implies a 3.5% RMS dispersion for a 86 mV signal. Due to the excellent linearity, the gain can be easily calibrated and off-line correction can be applied if needed. The S-curve measurement is also employed to extract the noise. Fig. 14 shows the input-referred noise expressed in terms of Equivalent Noise Charge (ENC) as a function of the detector capacitance. The slope of 10 e^-/pF matches well the one expected form computer simulations and theoretical calculations. A noise floor of 1500 e^- at zero detector

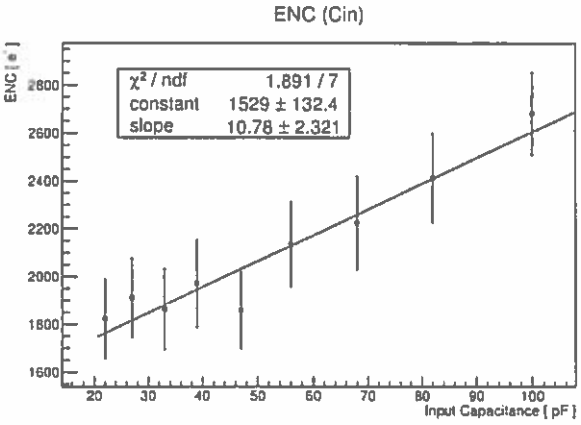

Fig. 14. ENC versus input capacitance.

capacitance is found. Possible candidates to explain the observed noise floor are switching noise due to on chip digital activity and common-mode noise due to non-optimal power supply rejection. More detailed studies on this issue are ongoing at the time of this writing. With the present noise performance, an ENC of 2500 electrons is obtained for a maximum detector capacitance of 100 pF. This allows to work with a 5 σ threshold of 2 fC, which is still sufficient for the proposed application. The Signal-to-Noise ratio would be about 10 for a silicon strip sensor with similar capacitance.