ALLEGATO N. 1 IV VERBALE

CONCORSO PER TITOLI ED ESAMI DI CUI AL BANDO N. 21797/2020 PER UN POSTO PER IL PROFILO PROFESSIONALE DI TECNOLOGO DI III LIVELLO PROFESSIONALE, PER ASSUNZIONE A TEMPO INDETERMINATO PRESSO LA SEZIONE DI PISA DELL'INFN.

ELENCO QUESITI PREDISPOSTI PER LA PROVA ORALE

TESTO n. 1

1. Come funziona la tecnica di Time-over-Threshold per l'integrazione di carica?
2. Quali sono le tecniche di compressione dei dati che possono essere utilizzate per ridurne la dimensione?

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In this chapter we turn our attention towards the design of semiconductor memory circuits. This includes the array design, sensing, and, finally, the operation of the memory cells themselves. The memories we look at in this chapter are termed random access memories or RAM because any bit of data can be accessed at any time. A block diagram of a RAM is shown in Fig. 16.1. At the intersection of a row line (a.k.a., word line) and a column line (a.k.a., a digit or bit line) is a memory cell. External to the memory array are

TESTO n. 2

1. Come funziona un Flash-ADC e quali vantaggi e limitazioni comporta rispetto ad altri sistemi di digitalizzazione del segnale?
2. Avendo da campionare un segnale analogico, quali sono le condizioni da rispettare affinché il segnale campionato e quello originale contengano le stesse informazioni?

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16.3.1 The SRAM Cell

The schematic and layout of a six-transistor SRAM memory cell is seen in Fig. 16.48. This is, as its name implies, static, meaning that as long as power is applied to the cell it will remember its contents (unlike the DRAM cell, which loses its memory after a short time). The basic cross-coupled inverter latch should be recognized in the topology. To access the cell, the word line goes high and turns on the access MOSFETs. The bit lines are driven in complementary directions with a "strong" driver for writing. When the word line goes low, the datum is latched in the cell.

TESTO n. 3

1. Discutere vantaggi e svantaggi di diverse architetture di convertitore digitale/analogico (DAC)
2. Discutere le principali architetture di memoria, i loro vantaggi e svantaggi a seconda dell'applicazione

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18.2 Multivibrator Circuits

Multivibrator circuits (Fig. 18.9) are circuits that employ positive feedback. The name "multivibrator" is a vestige from early-time electronics development (prior to the ubiquitous term "digital") where the circuits' outputs vibrate between two states. There are three types of multivibrators: astable, bistable, and monostable. Astable multivibrator circuits are unstable in either output (high or low) state. The oscillators that we have discussed are examples of astable multivibrators. The bistable multivibrator is stable in either the high or low state. Flip-flops and latches are examples of the bistable multivibrator. Monostable multivibrators are stable in a single state. Monostable multivibrators are also called one-shots. In this section we discuss the monostable and astable multivibrators. We distinguish the material in this section from the other material in the book by using resistor-capacitor time constants to set time intervals.

TESTO n. 4

1. Discutere il ruolo della capacità di controreazione in un preamplificatore di carica e collegarlo alla capacità del rivelatore
2. Discutere le architetture di readout in sistemi dotati di trigger

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Negative Voltages

The positive voltage pump uses n-channel MOSFETs, while the negative voltage pump, Fig. 18.35, uses p-channel MOSFETs. The reason for this comes from the requirement that the diode formed with the n+ (p+) implant used in the drain/source of the MOSFET combined with the p-substrate (n-well) does not become forward-biased. Forward biasing this parasitic diode is an *important concern* and is often the reason why some more exotic pump topologies can't be implemented. For example, in Fig. 18.35, we connect the well of the PMOS devices to ground instead of to their respective sources. Consider what would have happened had we connected the well to the source of the MOSFET. When the output voltage goes negative, the (n-type) well goes negative too. If the substrate (p-type) is at ground, this forward biases the n-well to substrate diode acting to clamp the output of the pump at a negative diode drop. While we could have left the bodies of the PMOS (the n-wells) tied to *VDD*, here we chose to connect them to ground so that the body effect wasn't so severe (a lower threshold voltage).

TESTO n. 5

1. Descrivere le possibili architetture di distribuzione della tensione ad un sistema di centinaia di rivelatori in un esperimento di alte energie.
2. Protocolli di comunicazione nei link cablati (ad es. I2C, SPI)

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The digital phase-locked loop, DPLL, is a circuit that is used frequently in modern integrated circuit design. Consider the waveform and block diagram of a communication system shown in Fig. 19.1. Digital data[1] is loaded into the shift register at the transmitting end. The data is shifted out sequentially to the transmitter output driver. At the receiving end, where the data may be analog (and, thus, without well-defined amplitudes) after passing through the communication channel, the receiver amplifies and changes the data back into digital logic levels. The next logical step in this sequence is to shift the data back into a shift register at the receiver and process the received data. However, the absence of a clock signal makes this difficult. The DPLL performs the function of generating a clock signal, which is locked or synchronized with the incoming signal. The generated clock signal of the receiver clocks the shift register and thus recovers the data. This application of a DPLL is often termed *a clock-recovery circuit* or *bit synchronization circuit.*

TESTO n. 6

1. Discutere i vantaggi e svantaggi della distribuzione di potenza usando l'alimentazione seriale (serial powering) e DC-DC converter
2. Discutere i tipi e le principali applicazioni di link ottici cablati

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Another source of potential distortion occurs when the receiver input data is regenerated into digital levels. This was discussed back in Sec. 18.3. Timing errors occur when the input data is not precisely sliced through its middle (see Fig. 18.12). What makes slicing the data correctly even more difficult is the fact that the amplitude response of the channel can change with time and the data pattern can affect the average level of the data. There are two solutions to this problem. The first uses a circuit (see Fig. 18.29) that determines the peak positive and negative input analog amplitudes, averages the values, and feeds back the result to the comparator in the decision-making circuit. The second method encodes the digital data so that the duty cycle of the resulting encoded data is 50%. The encoding increases the channel bandwidth for a constant data rate.

TESTO n. 7

1. Descrivere le tecniche di mitigazione degli effetti dovuti alla dose di radiazione integrata nella progettazione di circuiti microelettronici
2. Discutere i problemi legati alla progettazione e operazione di boards di back-end in un rack (cooling, potenze, noise acustico ecc)

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In the last chapter big resistors and capacitors were used to bias the circuits to the correct operating point, as seen in Fig. 21.21. The DC operating voltage on the gate of M1 (in Figs. 21.17 or 21.21) is extremely important when biasing the amplifier. If it's not at precisely the correct value, then the current sourced by M2 won't equal the current in M1 when both MOSFETs are operating in the saturation region.

The differential amplifier (*diff-amp*) is used on the input of an amplifier to allow input voltages to move around so that biasing of the gain stages isn't affected (that is, so it isn't a function of the input voltage). The diff-amp is a fundamental building block in CMOS analog integrated circuit design, and an understanding of its operation and design is extremely important. In this chapter we discuss three basic types of differential amplifiers: the source-coupled pair, the source cross-coupled pair, and the current differential amplifier.

TESTO n. 8

1. Descrivere le problematiche di Single Event Effects in circuiti microelettronici e le tecniche di mitigazione
2. Discutere i filtri di eliminazione del rumore elettronico fornendo alcuni esempi

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A general-use (ideal) voltage reference is a circuit used to generate a fixed voltage, V_{REF}, that is independent of the power supply voltage *VDD* (where $V_{REF} < VDD$), temperature, and process variations. In other words, the ideal reference voltage is independent of PVT. In some cases, we want to design a reference that varies with temperature. For example, if V_{REF} increases with temperature, Fig. 23.1a, we say that the reference voltage is *proportional to absolute temperature* or PTAT. If the reference voltage decreases with increasing temperature, Fig. 23.1b, the reference is said to be *complementary to absolute temperature* or CTAT. The PTAT and CTAT references can be used to design a voltage reference that changes very little with temperature called a *bandgap* reference. Unfortunately, the generation of PTAT and CTAT reference voltages requires using parasitic diodes. In a CMOS process, the electrical characteristics of the parasitic pn junctions are not monitored and controlled (like, say, the threshold voltage) during manufacturing. Therefore, if possible, the implementation of a reference voltage using MOSFET-resistor circuits is desirable.